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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/071,069	02/08/2002	Terry Lyon	10016630-1	3380

7590 05/07/2003

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EXAMINER	
MCLEAN-MAYO, KIMBERLY N	
ART UNIT	**PAPER NUMBER**
2187	2

DATE MAILED: 05/07/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/071,069	LYON, TERRY	
	Examiner	Art Unit	
	Kimberly N. McLean-Mayo	2187	

-- The MAILING DATE of this communication appears on the cover sheet with the c rrespondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 February 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The enclosed detailed action is in response to the Application submitted on February 8, 2002.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-3, 6-8 and 10-11 are rejected under 35 U.S.C. 102(e) as being anticipated by Steely, Jr. PGPUB: US 2002/0099913 A1).

Regarding claim 1, Steely discloses a unified tag memory coupled to be addressed by the tag index portion of the cache line address, the tag memory comprising at least one way specific address tag (Figure 3, comprised of sub-tags Reference 304 in Figure 3 for the L1 and L2 cache), at least one upper level valid flag (at least one of the valid bits in the upper level sub-tag memory)(Reference 418 in sub-tag 304 for L2 cache), and at least one way specific lower level flag (at least one of the valid bits in the lower level sub-tag memory)(Reference 418 in sub-tag 304 for L1 cache); at least one first comparator coupled to compare the high order part with the at least one way specific address tag and detect a match (Page 4, Section [0038], lines 7-10 – comparing function is performed by comparator(s)); a lower level hit logic coupled to determine a lower level cache hit when the at least one first comparator detects a match and the level flag

indicates a valid entry in the lower level cache (Page 4, Section [0038]; Figure 7A, References 702, 704, 706, 708 and 710 - logic within Reference 302 in Figure 3, in the L1 cache for performing the functions described in the cited sections); and an upper level hit logic coupled to determine a higher level cache hit when the at least one first comparator detects a match and high level valid flag is in a valid state (Page 4, Section [0039], Section [0039], lines 8-14; Figure 7C, References 730, 732, 734; Figure 7A, References 706, 708 and 710 - logic within Reference 302 in Figure 3, in the L2 cache for performing the functions described in the cited sections).

Regarding claims 2 and 6, Steely discloses the use of a set associative (Page 4, Section [0034], lines 12-16] and thus accordingly the system comprises a plurality (two or more) of way specific address tags and first comparators for multiple ways of associativity.

Regarding claim 3, Steely comprises cache coherency maintenance logic coupled to the tag memory subsystem (Page 1, Section [0011 - 0013]; Page 3, Section [0026]; Page 4, Section [0040-0041] – directory based cache coherency).

Regarding claim 7, Steely discloses a lower level cache data memory coupled to provide data to the processor port on a lower level cache hit (Page 4, Section [0038] – L1 cache hit); an upper level cache data memory coupled to provide data to the processor port on an upper level cache hit (Figure 7C, References 730, 732, 734; Figure 7A, References 706, 708, 710; Figure 7C, Reference 744); unified tag memory coupled to be addressed by the tag index portion of the cache line address, the tag memory comprising at least one way specific address tag (Figure 3,

comprised of sub-tags Reference 304 in Figure 3 for the L1 and L2 cache), at least one upper level valid flag (at least one of the valid bits in the upper level sub-tag memory)(Reference 418 in sub-tag 304 for L2 cache), and at least one way specific lower level flag (at least one of the valid bits in the lower level sub-tag memory)(Reference 418 in sub-tag 304 for L1 cache); at least one first comparator coupled to compare the high order part with the at least one way specific address tag and detect a match (Page 4, Section [0038], lines 7-10 – comparing function is performed by comparator(s)); a lower level hit logic coupled to determine a lower level cache hit when the at least one first comparator detects a match and the level flag indicates a valid entry in the lower level cache (Page 4, Section [0038]; Figure 7A, References 702, 704, 706, 708 and 710 - logic within Reference 302 in Figure 3, in the L1 cache for performing the functions described in the cited sections); and an upper level hit logic coupled to determine a higher level cache hit when the at least one first comparator detects a match and high level valid flag is in a valid state (Page 4, Section [0039], Section [0039], lines 8-14; Figure 7C, References 730, 732, 734; Figure 7A, References 706, 708 and 710 - logic within Reference 302 in Figure 3, in the L2 cache for performing the functions described in the cited sections).

Regarding claims 8 and 11, Steely discloses the higher level valid flag comprising a plurality of higher level valid flags for indicating the validity of data in a line of a superline (wherein a superline is comprised of each sub-line, having a same address, in each set in the upper level cache data memory and wherein each valid flag for each line in the superline is a superline segment flag)(Steely discloses the use of a set associative (Page 4, Section [0034], lines 12-16]

and thus accordingly the system comprises a plurality of higher level valid flags, [one for each way in the higher level cache data memory] and superlines).

Regarding claim 10, Steely comprises cache coherency maintenance logic coupled to the tag memory subsystem (Page 1, Section [0011 - 0013]; Page 3, Section [0026]; Page 4, Section [0040-0041] – directory based cache coherency).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Steely (PGPUB: 2002/0099913 A1).

Steely does not explicitly disclose cache coherency logic as cache snoop logic. However, it is well known in the art to use snoop logic as a simple and efficient means to perform cache coherency functions in system in which the processing elements are all coupled to a common bus. Steely discloses in Figure 1, all the processing elements [nodes] coupled to a central interconnect, Reference 104 and thus it would have been obvious to one of ordinary skill in the art to provide snoop logic to perform cache coherency maintenance in the system taught by Steely for the desirable purpose of simpler design and efficiency.

6. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Steely (PGPUB: 2002/0099913 A1).

Steely does not explicitly disclose the lower level flag indicating a way of storage in lower level data memory at which cache data may be located. However, way prediction is well known in the art for providing an indication of a way of storage in the cache where data may be located. This feature is known for improving the performance of the cache by quickly providing requested data when a correct prediction occurs. Hence, it would have been obvious to one of ordinary skill in the art to provide this feature in Steely's system for the desirable purpose of improved performance.

7. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Steely (PGPUB: 2002/0099913 A1) as applied to claim 7 above and further in view of Chaudhry et al. (PGPUB: US 2002/0152359 A1).

Steely discloses the lower level flag field of the unified cache tag subsystem comprising a plurality of lower level flags (Steely discloses the use of a set associative (Page 4, Section [0034], lines 12-16 and thus accordingly the system comprises a plurality of lower level valid flags, [one for each way in the lower level cache data memory]). However, Steely does not disclose a cache line in the lower level cache smaller than a cache line of the upper level cache data memory, wherein the lower level data cache has fewer ways of storage than the upper level cache data memory, wherein the lower level flag field of the unified cache tag subsystem indicates ways of storage in lower level cache data memory where corresponding data is located in the lower level cache data memory. Chaudhry teaches a cache line (line comprised of each

sub-line in each way of the lower level cache) in the lower level cache smaller than a cache line of the upper level cache data memory, wherein the lower level data cache has fewer ways of storage than the upper level cache data memory (Page 3, Section [0043] – L1 cache is 4 way set associative; Page 3, Section [0041] – L2 cache is 8 way set associative; the cache line in the L1 cache is comprised of less ways and thus comprises a smaller amount of data than a L2 cache line). These features taught by Chaudhry are provided to obtain a desired level of performance from the cache system. Caches can be implemented in many organizations depending upon the desired objectives and requirements of a system. Hence, it would have been obvious to one of ordinary skill in the art to use the features taught by Chaudhry in the system taught by Steely for the desirable purpose of obtaining a level of performance afforded by using the specific cache organization.

8. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Steely (PGPUB: 2002/0099913 A1) as applied to claim 7 above and further in view of Syed et al. (PGPUB: US 2002/0108021 A1).

Steely does not explicitly disclose disabling specific ways of storage. However, Syed teaches the concept of disabling ways of storage (with respect to the processor) (Abstract; Page 8, Section [0083]) to provide concurrent access to the cache thereby improving the throughput of the system. Hence, it would have been obvious to one of ordinary skill in the art to use the teachings of Syed with the system of Steely for the desirable purpose of improved throughput.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Lovett – USPN: 5,802,578 – combined tag.

Lyon et al. – USPN : 6,427,188 – parallel access to L1 and L2 tags.

Aichelmann – USPN: 4,823,259 – cache superlines.

Kumar – USPN: 6,247,094 – cache way prediction.

Tran – USPN: 6,115,792 – cache way prediction.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kimberly N. McLean-Mayo whose telephone number is 703-308-9592. The examiner can normally be reached on M-F (9:00 - 6:30) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on 703-308-1756. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7329 for regular communications and 703-746-7240 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-2100.

Kimberly N. McLean-Mayo
Examiner
Art Unit 2187

KNM

May 3, 2003